REMARKS

Pending Claims

Claims 12-26 are currently pending. Claims 1-11 were previously canceled. Claim 24 has been amended to correct a typographical error. No new matter is added.

Amendments to the Specification

The Examiner has objected to the Abstract for containing more than 150 words. Accordingly, Applicant has submitted a new Abstract containing exactly 150 words. As this Abstract is based on the language of claim 12, no new matter is added. Applicant respectfully requests that the Examiner reconsider and withdraw the objection.

Objections to the Claims

The Examiner has objected to claims 16 and 24 for containing informalities.

With regard to claim 24, the Examiner notes that the term "recover circuit" should be changed to "recovery circuit." Appropriate correction has been made.

With regard to claim 16, the Examiner objects to the use of the term "therebetween" and suggests changing this to "there between." However, Applicant respectfully submits that "therebetween" is the correct term to use. The relevant portion of claim 16 reads:

> a first phase detector circuit receiving the clock signal output from said voltage-controlled oscillator circuit and said reference clock signal to detect the phase difference ***therebetween***,

the term "therebetween" indicating that the first phase detector circuit receives the clock signal output from the voltage-controlled oscillator circuit as well as the reference clock signal, and detects the phase difference between the two signals. Applicant respectfully notes that the US Patent Office itself uses this term, for example in the title of Class 301 Land Vehicles: Wheels and Axles, Subclass 36.3 "Dual Wheels With Wear-Preventing Means ***Therebetween***." Applicant submits that "therebetween" is a valid term and is used correctly

in claim 16, and respectfully requests that the Examiner reconsider and withdraw the objection to claim 16.

Applicant has made the change to claim 24 as suggested by the Examiner, but Applicant respectfully submits that claim 16 is correct as written. Applicant respectfully requests that the Examiner reconsider and withdraw the objections to claims 16 and 24.

Rejections Under 35 U.S.C. § 103

Claims 12-16 and 24-26 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of what the Examiner has termed the Applicant Admitted Prior Art ("AAPA") in view of Miyashita et al. (USP 5,610,954). In addition, claims 19-22 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Yonekura et al. (USP 5,761,617). Further, claims 17-18 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Anumula et al. (USP 6,566,967). Finally, claim 23 stands rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Yonekura et al. (USP 5,761,617). However, in view of the arguments presented herein, Applicant respectfully submits that the rejections have been traversed and request that the rejections be reconsidered and withdrawn.

Claims 12-26 are not obvious because the combination of cited references fails to teach or suggest all of the elements of the claims. Furthermore, in rejecting the claims the Examiner has failed to consider whether the invention "as a whole" would have been obvious in view of the art, and instead has impermissibly conducted an analysis on an element-by-element basis: "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." MPEP 2141.02 (Emphasis in original).

The Examiner has identified sub-portions of the phase-locked loop circuit shown in Figure 7 of Miyashita et al. as corresponding to particular claim elements, without regard to the context in which these circuit elements are disclosed in the Miyashita et al. reference and

without citing any teaching which would have led one skilled in the art to combine the elements to produce the claimed clock and data recovery circuit. In particular, the elements identified by the Examiner in Figure 7 of Miyashita et al., namely elements 21A, 21B, and 22B, are in fact part of a phase detector 20 which in turn is a component of the phase-locked loop circuit that is the subject of Figure 7. While embodiments of the clock and data recovery circuit of the present invention include a phase-locked loop (PLL), the Examiner does not apply the elements from Miyashita et al. as part of a PLL but instead argues that PLL elements would have been used in other ways, in combination with the circuit shown in the AAPA, to produced the claimed circuits. However, the Examiner fails to cite any teaching which would have led one skilled in the art to make the particular combinations of elements recited in the claims.

For example, the Examiner argues that the AAPA discloses "a phase synchronization loop" and "a phase shift circuit" as recited in independent claim 12. The Examiner further argues that Miyashita et al. supplies the deficiencies of the AAPA by teaching the claimed "discriminator circuit" and "phase detector circuit," where "the clock signal, output from said phase shift circuit, [is] supplied as said clock signal for discrimination to said discriminator circuit." In particular the Examiner's position is that elements 21A and 21B of Miyashita et al. serve as the claimed "discriminator circuit" and that element 22A serves as the "phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said input data signal" as recited in claim 12.

The output of the combination of elements 21A and 21B of Miyashita et al., which the Examiner argues is equivalent to the claimed discriminator, is the "RDATA" signal, which is inconsistent with element 22A serving as the phase detector. As recited in claim 12, the phase detector compares the output of the discriminator to the input data signal. However, the inputs to element 22A are the input data signal "DATA IN" and the output of element 21A, "QA," and not the "RDATA" output from the combined element 21A/21B that the Examiner has characterized as being equivalent to the discriminator.

In addition, claim 12 recites that the output of the "phase detector circuit" is used by the "phase shift circuit" to shift the phase of the clock signal that is output from the oscillator. However, the output of element 22A in Miyashita et al., along with the output of element 22B, is fed into operational amplifier 32 to produce a variable voltage which is fed into the

VCO 50 to control the frequency of the clock output: "The voltage controlled oscillator (VCO) 50 outputs the complementary clocks CLK and *CLK whose frequency is proportion to an output voltage of the loop filter 30." See Miyashita et al. at col. 14, lines 47-49. There is no teaching in the cited references which would have directed one skilled in the art to combine the PLL circuit elements in Figure 7 of Miyashita et al. with the circuits discussed in the AAPA to produce the claimed clock and data recovery circuit.

Thus, the Examiner has rejected the claims by taking several circuit elements from Miyashita et al. out of context and combining them with information from the AAPA in a manner that is internally inconsistent and also inconsistent with the original purpose of the circuit elements in Miyashita et al. Besides the fact that not all of the elements of the claims are taught or suggested by the combination of references, there is nothing in either of the references or in the general knowledge of one skilled in the art that would have led a skilled artisan to combine the circuit elements so as to produce the claimed circuit. For at least these reasons, claim 12 is not rendered obvious by the combination of the AAPA in view of Miyashita et al. and is thus allowable.

With regard to independent claims 13 and 15, each of these claims recites among other elements "a second feedback loop including a discriminator circuit supplied with said received data signal, and a second phase detector circuit for detecting the phase difference between the data signal, discriminated and output by said discriminator circuit, and said received data signal." However, because the combined references fail to teach all of the elements of claims 13 and 15 and because the Examiner has cited individual elements from the references out of context and has failed to consider "whether the claimed invention as a whole would have been obvious," claims 13 and 15 are not obvious over the AAPA in view of Miyashita et al.

The Examiner argues that the AAPA teaches a second feedback loop which includes a discriminator circuit. However, the discriminator 904 shown in the circuit of Figure 11 of the present application, which is part of the AAPA cited by the Examiner, is not in fact part of a loop, nor does the feedback loop (Figure 11, clock delay means 903) from the AAPA that is cited by the Examiner include a discriminator. In addition, elements 21A/21B of Miyashita et al., which the Examiner identifies as being equivalent to the claimed discriminator circuit, are not part of a loop with a phase detector circuit which detects the phase difference between the data signal and the output of the discriminator, as recited in claims 13 and 15. Instead,

element 22A, which the Examiner argues is equivalent to the second phase detector circuit, has as its inputs the input data signal and the signal QA, which is the output of element 21A.

As with claim 12, the Examiner has rejected independent claims 13 and 15 by comparing individual elements of the AAPA and Miyashita et al. to individual elements of the claims in isolation and without citing any teaching in the references or in the knowledge of one skilled in the art which would have led one skilled in the art to combine the elements from the references in order to produce the claimed clock and data recovery circuit. Furthermore, the combination of references fails to teach or suggest all of the elements of claims 13 and 15. For at least these reasons, claims 13 and 15 are not rendered obvious by the combination of the AAPA in view of Miyashita et al. and are thus allowable.

Overall, the claimed invention includes significant differences from the cited references. For example, the feedback loop controlling the phase shift circuit is separate from the control terminal of the VCO output, as recited, e.g., in claims 14, 16, and 18. As can be seen, e.g., in Figure 1 of the present application, without directly controlling the VCO output, the phase shifter 108 is only controlled by the second feedback loop, to determine the correct output data signal 106.

On the other hand, the cited references disclose that the clock data is recovered by feedback of the control signal to the control terminal of the VCO output. Since Figure 11 of the AAPA does not have the specified claimed formulation of the present invention (including, e.g., "a phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said input data signal," as recited in claim 12), it cannot perform automatic feedback control of the phase shift as a function of the output data.

The remaining claims are allowable because each depends from one of the allowable independent claims 12, 13, and 15, and because each dependent claim recites additional patentable subject matter.

CONCLUSION

In view of the remarks and amendments presented herein, reconsideration and withdrawal of the pending rejections and allowance of the claims are respectfully requested. The Examiner is strongly encouraged to contact the undersigned at the phone number below should any issues remain with respect to the application.

Respectfully submitted,

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